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# Am25LS2519

Quad Register with Two Independently Controlled Three-State Outputs

## DISTINCTIVE CHARACTERISTICS

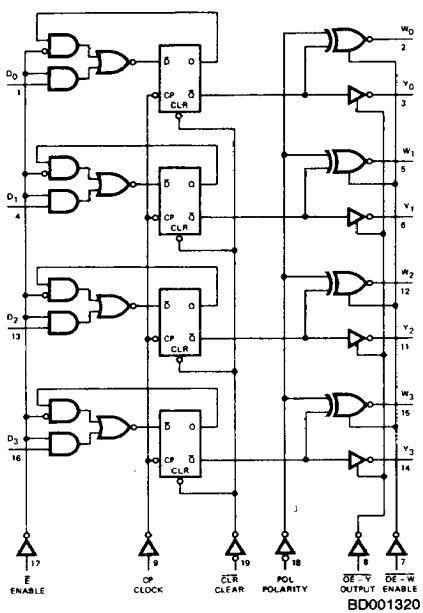
- Two sets of fully buffered three-state outputs
- Four D-type flip-flops
- Polarity control on W outputs
- Buffered common clock enable
- Buffered common asynchronous clear
- Separate buffered common output enable for each set of outputs

## GENERAL DESCRIPTION

The Am25LS2519 consists of four D-type flip-flops with a buffered common clock enable. Information meeting the set-up and hold time requirements on the D inputs is transferred to the flip-flop outputs on the LOW-to-HIGH transition of the clock. Data on the Q outputs of the flip-flops is enabled at the three-state outputs when the output control ($\overline{OE}$) input is LOW. When the appropriate $\overline{OE}$ input is HIGH, the outputs are in the high impedance state. Two independent sets of outputs – W and Y – are provided such that the register can simultaneously and independently drive two buses. One set of outputs contains a polarity control such that the outputs can either be inverting or non-inverting.

The device also features an active LOW asynchronous clear. When the clear input is LOW, the Q output of the internal flip-flops are forced LOW independent of the other inputs. The Am25LS2519 is packaged in a space saving (0.3-inch row spacing) 20-pin package.

## BLOCK DIAGRAM

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## RELATED PRODUCTS

| Part No. | Description |
|---|---|
| Am25S18, Am2918 | Quad D Register |
| Am25LS2518 | Quad D Register |

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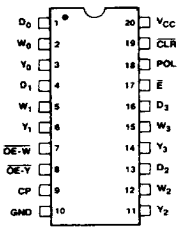
## CONNECTION DIAGRAM
Top View

D-20-1

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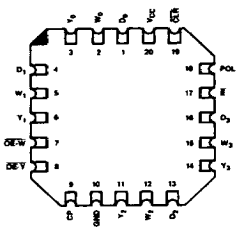
L-20-1



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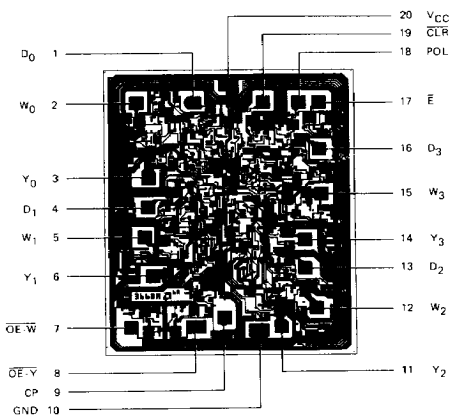
Note: Pin 1 is marked for orientation

## METALLIZATION AND PAD LAYOUT




**DIE SIZE 0.083" x 0.099"**

## ORDERING INFORMATION

AMD products are available in several packages and operating ranges. The order number is formed by a combination of the following: Device number, speed option (if applicable), package type, operating range and screening option (if desired).

**Am25LS2519** **D** **C** **B**

- **B** — Screening Option
  - Blank – Standard processing
  - B – Burn-in
- **C** — Temperature (See Operating Range)
  - C – Commercial (0°C to +70°C)
  - M – Military (–55°C to +125°C)
- **D** — Package
  - D – 20-pin CERDIP
  - F – 20-pin flatpak
  - L – 20-pin leadless chip carrier
  - P – 20-pin plastic DIP
  - X – Dice
- **Am25LS2519** — Device type: Quad D Register

| Valid Combinations | |
|---|---|
| Am25LS2519 | PC<br>DC, DM<br>FM<br>LC, LM<br>XC, XM |

**Valid Combinations**

Consult the AMD sales office in your area to determine if a device is currently available in the combination you wish.

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## PIN DESCRIPTION

| Pin No. | Name | I/O | Description |
|---|---|---|---|
| | $D_i$ | I | Any of the four D flip-flop data lines. |
| 17 | $\overline{E}$ | I | Clock Enable. When LOW, the data is entered into the register on the next clock LOW-to-HIGH transition. When HIGH, the data in the register remains unchanged, regardless of the data in. |
| 9 | CP | I | Clock Pulse. Data is entered into the register on the LOW-to-HIGH transition. |
| 7, 8 | $\overline{OE}$-W, $\overline{OE}$-Y | O | Output Enable. When $\overline{OE}$ is LOW, the register is enable to the output. When HIGH, the output is in the high-impedance state. The $\overline{OE}$-W controls the W set of outputs, and $\overline{OE}$-Y controls the Y set. |
| | $Y_i$ | O | Any of the four non-inverting three-state output lines. |
| | $W_i$ | O | Any of the four three-state outputs with polarity control. |
| 18 | POL | O | Polarity Control. The $W_i$ outputs will be non-inverting when POL is LOW, and when it is HIGH, the outputs are inverting. |
| 19 | $\overline{CLR}$ | I | Asynchronous Clear. When $\overline{CLR}$ is LOW, the internal Q flip-flops are reset to LOW. |

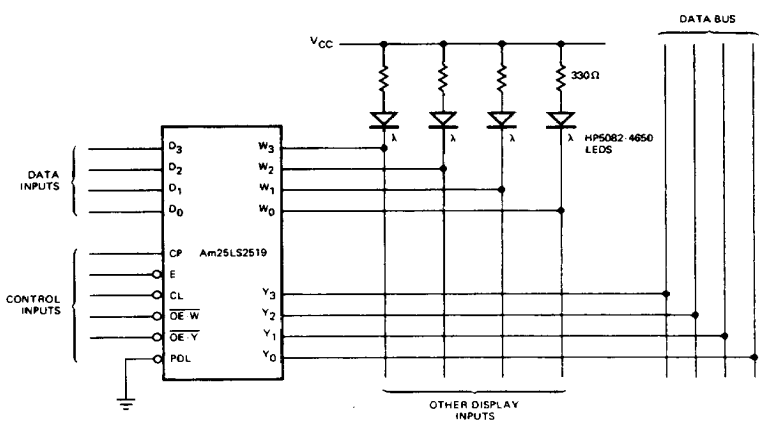
## FUNCTION TABLE

| FUNCTION | INPUTS | | | | | | | INTERNAL | OUTPUTS | |
|---|---|---|---|---|---|---|---|---|---|---|
| | CP | $D_i$ | $\overline{E}$ | $\overline{CLR}$ | POL | $\overline{OE}$-W | $\overline{OE}$-Y | Q | $W_i$ | $Y_i$ |
| Output Three-State Control | X | X | X | X | X | H | L | NC | Z | Enabled |
| | X | X | X | X | X | L | H | NC | Enabled | Z |
| | X | X | X | X | X | H | H | NC | Z | Z |
| | X | X | X | X | X | L | L | NC | Enabled | Enabled |
| $W_i$ Polarity | X | X | X | X | L | L | L | NC | Non-Inverting | Non-Inverting |
| | X | X | X | X | H | L | L | NC | Inverting | Non-Inverting |
| Asynchronous Clear | X | X | X | L | L | L | L | L | L | L |
| | X | X | X | L | H | L | L | L | H | L |
| Clock Enabled | ↑ | X | H | H | X | X | X | NC | NC | NC |
| | ↑ | L | L | H | L | L | L | L | L | L |
| | ↑ | L | L | H | H | L | L | L | H | L |
| | ↑ | H | L | H | L | L | L | H | H | H |
| | ↑ | H | L | H | H | L | L | H | L | H |

L = LOW
H = HIGH
Z = High-Impedance

X = Don't Care
NC = No Change
↑ = LOW to HIGH Transition

## APPLICATION




Convenient Register Content Monitor or Test Point

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## ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65°C to +150°C
Ambient Temperature Under Bias ..... −55°C to +125°C
Supply Voltage to Ground Potential
Continuous ..... −0.5V to +7.0V
DC Voltage Applied to Outputs For
High Output State ..... −0.5V to +$V_{CC}$ max
DC Input Voltage ..... −0.5V to +7.0V
DC Output Current, Into Outputs ..... 30mA
DC Input Current ..... −30mA to +5.0mA

*Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.*

## OPERATING RANGES

Commercial (C) Devices
Temperature ..... 0°C to +70°C
Supply Voltage ..... +4.75V to +5.25V

Military (M) Devices
Temperature ..... −55°C to +125°C
Supply Voltage ..... +4.5V to +5.5V

*Operating ranges define those limits over which the functionality of the device is guaranteed.*

## DC CHARACTERISTICS over operating range unless otherwise specified

| Parameters | Description | Test Conditions (Note 2) | | Min | Typ (Note 1) | Max | Units |
|---|---|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH Voltage | $V_{CC}$ = MIN, $V_{IN}$ = $V_{IH}$ or $V_{IL}$ | MIL, $I_{OH}$ = −1.0mA | 2.4 | 3.4 | | Volts |
| | | | COM'L, $I_{OH}$ = −2.6mA | 2.4 | 3.4 | | |
| $V_{OL}$ | Output LOW Voltage | $V_{CC}$ = MIN, $V_{IN}$ = $V_{IH}$ or $V_{IL}$ | $I_{OL}$ = 4.0 mA | | | 0.4 | Volts |
| | | | $I_{OL}$ = 8.0mA | | | 0.45 | |
| | | | $I_{OL}$ = 12mA | | | 0.5 | |
| $V_{IH}$ | Input HIGH Level | Guaranteed input logical HIGH voltage for all inputs | | 2.0 | | | Volts |
| $V_{IL}$ | Input LOW Level | Guaranteed input logical LOW voltage for all inputs. | MIL | | | 0.7 | Volts |
| | | | COM'L | | | 0.8 | |
| $V_I$ | Input Clamp Voltage | $V_{CC}$ = MIN, $I_{IN}$ = −18mA | | | | −1.5 | Volts |
| $I_{IL}$ | Input LOW Current | $V_{CC}$ = MAX, $V_{IN}$ = 0.4V | | | | −0.36 | mA |
| $I_{IH}$ | Input HIGH Current | $V_{CC}$ = MAX, $V_{IN}$ = 2.7V | | | | 20 | μA |
| $I_I$ | Input HIGH Current | $V_{CC}$ = MAX, $V_{IN}$ = 7.0V | | | | 0.1 | mA |
| $I_{OZ}$ | Off-State (High-Impedance) Output Current | $V_{CC}$ = MAX | $V_O$ = 0.4V | | | −20 | μA |
| | | | $V_O$ = 2.4V | | | 20 | |
| $I_{SC}$ | Output Short Circuit Current (Note 3) | $V_{CC}$ = MAX | | −15 | | −85 | mA |
| $I_{CC}$ | Power Supply Current (Note 4) | $V_{CC}$ = MAX | MIL | | 24 | 36 | mA |
| | | | COM'L | | 24 | 39 | |

Notes: 1. Typical limits are at $V_{CC}$ = 5.0V, 25°C ambient and maximum loading.
2. For conditions shown as MIN or MAX, use the appropriate value specified under Operating Ranges for the applicable device type.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. Inputs grounded; outputs open.

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## SWITCHING CHARACTERISTICS ($T_A$ = +25°C, $V_{CC}$ = 5.0V)

| Parameters | Description | | Test Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|---|
| $t_{PHL}$ | Clock to $Y_i$ | | $C_L$ = 15pF<br>$R_L$ = 2.0kΩ | | 22 | 33 | ns |
| $t_{PHL}$ | | | | | 20 | 30 | |
| $t_{PLH}$ | Clock to $W_i$ (Either Polarity) | | | | 24 | 36 | ns |
| $t_{PHL}$ | | | | | 24 | 36 | |
| $t_{PHL}$ | Clear to $Y_i$ | | | | 29 | 43 | ns |
| $t_{PLH}$ | Clear to $W_i$ | | | | 25 | 37 | ns |
| $t_{PHL}$ | | | | | 30 | 45 | |
| $t_{PLH}$ | Polarity to $W_i$ | | | | 23 | 34 | ns |
| $t_{PHL}$ | | | | | 25 | 37 | |
| $t_{pw}$ | Clear | | | 18 | | | ns |
| $t_{pw}$ | Clock Pulse Width | LOW | | 15 | | | ns |
| | | HIGH | | 18 | | | |
| $t_s$ | Data | | | 15 | | | ns |
| $t_h$ | Data | | | 5 | | | ns |
| $t_s$ | Data Enable | | | 20 | | | ns |
| $t_h$ | Data Enable | | | 0 | | | ns |
| $t_s$ | Set-up Time, Clear Recovery (Inactive) to clock | | | 20 | 15 | | ns |
| $t_{ZH}$ | Output Enable to W or Y | | | | 11 | 17 | ns |
| $t_{ZL}$ | | | | | 13 | 20 | |
| $t_{HZ}$ | Output Enable to W or Y | | $C_L$ = 5.0pF<br>$R_L$ = 2.0kΩ | | 13 | 20 | ns |
| $t_{LZ}$ | | | | | 11 | 17 | |
| $f_{max}$ | Maximum Clock Frequency (Note 1) | | $C_L$ = 15pF<br>$R_L$ = 2.0kΩ | 35 | 45 | | MHz |

Note 1. Per industry convention, $f_{max}$ is the worst case value of the maximum device operating frequency with no constraints on $t_r$, $t_f$, pulse width or duty cycle.

## SWITCHING CHARACTERISTICS over operating range unless otherwise specified*

| Parameters | Description | | Test Conditions | COMMERCIAL Am25LS2519 | | MILITARY Am25LS2519 | | Units |
|---|---|---|---|---|---|---|---|---|
| | | | | Min | Max | Min | Max | |
| $t_{PLH}$ | Clock to $Y_i$ | | $C_L$ = 50pF<br>$R_L$ = 2.0kΩ | | 39 | | 42 | ns |
| $t_{PHL}$ | | | | | 39 | | 45 | |
| $t_{PLH}$ | Clock to $W_i$ (Either Polarity) | | | | 41 | | 43 | ns |
| $t_{PHL}$ | | | | | 44 | | 48 | |
| $t_{PHL}$ | Clear to $Y_i$ | | | | 52 | | 58 | ns |
| $t_{PLH}$ | Clear to $W_i$ | | | | 42 | | 43 | ns |
| $t_{PHL}$ | | | | | 51 | | 53 | |
| $t_{PLH}$ | Polarity to $W_i$ | | | | 41 | | 45 | ns |
| $t_{PHL}$ | | | | | 42 | | 44 | |
| $t_{pw}$ | Clear | | | 20 | | 20 | | ns |
| $t_{pw}$ | Clock | LOW | | 20 | | 20 | | ns |
| | | HIGH | | 20 | | 20 | | |
| $t_s$ | Data | | | 15 | | 15 | | ns |
| $t_h$ | Data | | | 10 | | 10 | | ns |
| $t_s$ | Data Enable | | | 25 | | 25 | | ns |
| $t_h$ | Data Enable | | | 0 | | 0 | | ns |
| $t_s$ | Set-up Time, Clear Recovery (Inactive) to Clock | | | 23 | | 24 | | ns |
| $t_{ZH}$ | Output Enable to $W_i$ or $Y_i$ | | | | 24 | | 27 | |
| $t_{ZL}$ | | | | | 29 | | 35 | |
| $t_{HZ}$ | Output Enable to $W_i$ or $Y_i$ | | $C_L$ = 5.0pF<br>$R_L$ = 2.0kΩ | | 33 | | 45 | ns |
| $t_{LZ}$ | | | | | 22 | | 26 | |
| $f_{max}$ | Maximum Clock Frequency (Note 1) | | $C_L$ = 5.0pF<br>$R_L$ = 2.0kΩ | 30 | | 25 | | MHz |

*AC performance over the operating temperature range is guaranteed by testing defined in Group A, Subgroup 9.

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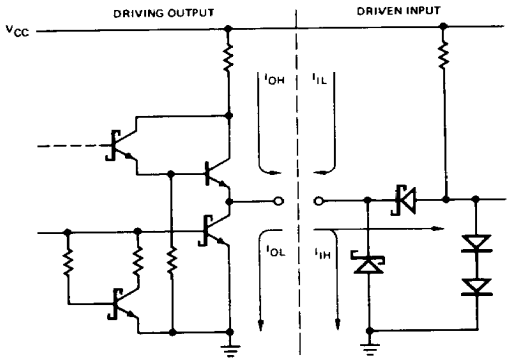
## Am25LS2519
## LOW-POWER SCHOTTKY INPUT/OUTPUT CURRENT INTERFACE CONDITIONS

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Note: Actual current flow direction shown.



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